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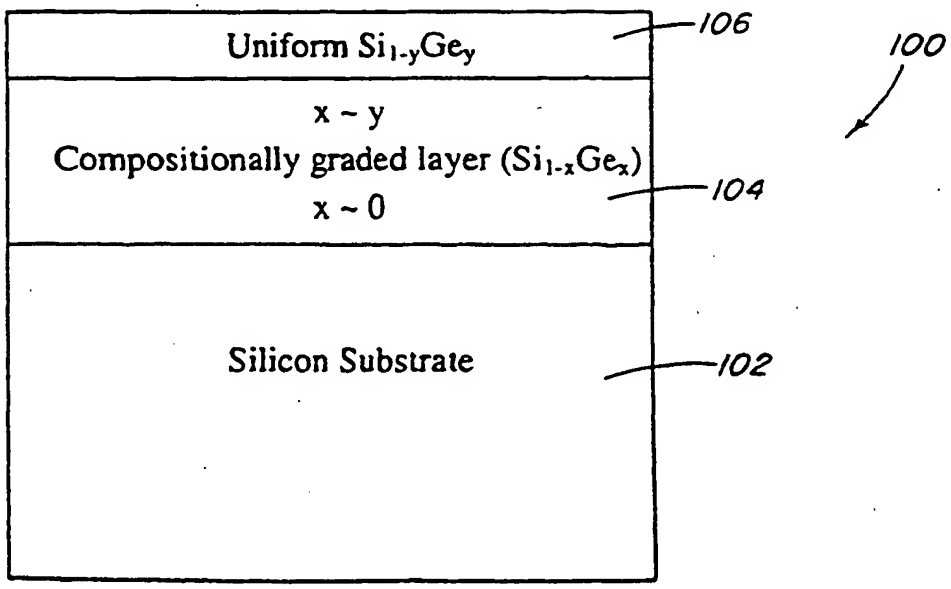

(57) Abstract: Structures and methods for fabricating high speed digital, analog, and combined digital/analog systems using planarized relaxed SiGe as the materials platform. The relaxed SiGe allows for a plethora of strained Si layers that possess enhanced electronic properties. By allowing the MOSFET channel to be either at the surface or buried, one can create high-speed digital and/or analog circuits. The planarization before the device epitaxial layers are deposited ensures a flat surface for state-of-the-art lithography.

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RELAXED SILICON GERMANIUM PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS

PRIORITY INFORMATION

This application claims priority from U.S. Patent Applications Nos. 09/906,200 and 09/906,201 both filed on July 16, 2001, which claim priority to U.S. provisional application Ser. No. 60/273,112 filed March 2, 2001.

BACKGROUND OF THE INVENTION

The invention relates to the field of relaxed SiGe platforms for high speed CMOS electronics and high speed analog circuits.

Si CMOS as a platform for digital integrated circuits has progressed predictably through the industry roadmap. The progress is created through device miniaturization, leading to higher performance, greater reliability, and lower cost. However, new bottlenecks in data flow are appearing as the interconnection hierarchy is expanded. Although digital integrated circuits have progressed at unprecedented rates, analog circuitry has hardly progressed at all. Furthermore, it appears that in the near future, serious economic and technological issues will confront the progress of digital integrated circuits.

The digital and communication chip markets need an enhancement to Si CMOS and the maturing roadmap. One promising candidate material that improves digital integrated circuit technology and introduces new analog integrated circuit possibilities is relaxed SiGe material on Si substrates. Relaxed SiGe alloys on Si can have thin layers of Si deposited on them, creating tension in the thin Si layers. Tensile Si layers have many advantageous properties for the basic device in integrated circuits, the metal-oxide field effect transistor (MOSFET). First, placing Si in tension increases the mobility of electrons moving parallel to the surface of the wafer, thus increasing the frequency of operation of the MOSFET and the associated circuit. Second, the band offset between the relaxed SiGe and the tensile Si will confine electrons in the Si layer. Therefore, in an electron channel device (n-channel), the channel can be removed from the surface or 'buried'. This ability to spatially separate the charge carriers from scattering centers such as ionized impurities and the 'rough' oxide interface enables the production of low noise, high performance analog devices and circuits.

A key development in this field was the invention of relaxed SiGe buffers with low

threading dislocation densities. The key background inventions in this area are described in U.S. Pat. No. 5,442,205 issued to Brasen et al. and U.S. Pat. No. 6,107,653 issued to Fitzgerald. These patents define the current best methods of fabricating high quality relaxed SiGe.

. . . . Novel device structures in research laboratories have been fabricated on early, primitive versions of the relaxed buffer. For example, strained Si, surface channel nMOSFETs have been created that show enhancements of over 60% in intrinsic g_m with electron mobility increases of over 75% (Rim et al, IEDM 98 Tech. Dig. p. 707). Strained Si, buried channel devices demonstrating high transconductance and high mobility have also been fabricated (U. Konig, MRS Symposium Proceedings 533, 3 (1998)). Unfortunately, these devices possess a variety of problems with respect to commercialization. First, the material quality that is generally available is insufficient for practical utilization, since the surface of SiGe on Si becomes very rough as the material is relaxed via dislocation introduction. These dislocations are essential in the growth of relaxed SiGe layers on Si since they compensate for the stress induced by the lattice mismatch between the materials. For more than 10 years, researchers have tried to intrinsically control the surface morphology through epitaxial growth, but since the stress fields from the misfit dislocations affect the growth front, no intrinsic epitaxial solution is possible. The invention describes a method of planarization and regrowth that allows all devices on relaxed SiGe to possess a significantly flatter surface. This reduction in surface roughness increases the yield for fine-line lithography, thus enabling the manufacture of strained Si devices.

A second problem with the strained Si devices made to date is that researchers have been concentrating on devices optimized for very different applications. The surface channel devices have been explored to enhance conventional MOSFET devices, whereas the buried channel devices have been constructed in ways that mimic the buried channel devices previously available only in III-V materials systems, like AlGaAs/GaAs. Recognizing that the Si manufacturing infrastructure needs a materials platform that is compatible with Si, scalable, and capable of being used in the plethora of Si integrated circuit applications, the disclosed invention provides a platform that allows both the enhancement of circuits based on Si CMOS, as well as the fabrication of analog circuits. Thus, high performance analog or digital systems can be designed with this platform. An additional advantage is that both types of circuits can be fabricated in the CMOS process, and therefore a combined, integrated digital/analog system can be designed as a single-chip solution.

With these advanced SiGe material platforms, it is now possible to provide a variety of device and circuit topologies that take advantage of this new materials system. Exemplary embodiments of the invention describe structures and methods to fabricate advanced strained-layer Si devices, and structures and methods to create circuits based on a multiplicity of devices, all fabricated from the same starting material platform. Starting from the same material platform is key to minimizing cost as well as to allowing as many circuit topologies to be built on this platform as possible.

SUMMARY OF THE INVENTION

Accordingly, the invention provides a material platform of planarized relaxed SiGe with regrown device layers. The planarization and regrowth strategy allows device layers to have minimal surface roughness as compared to strategies in which device layers are grown without planarization. This planarized and regrown platform is a host for strained Si devices that can possess optimal characteristics for both digital and analog circuits. Structures and processes are described that allow for the fabrication of high performance digital logic or analog circuits, but the same structure can be used to host a combination of digital and analog circuits, forming a single system-on-chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a structure including a relaxed SiGe layer epitaxially grown on a Si substrate;

FIG. 2 is a schematic block diagram of an exemplary structure showing that the origin of the crosshatch pattern is the stress fields from injected misfit dislocations;

FIG. 3 is a table showing surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates;

FIGs. 4A–4D show an exemplary process flow and resulting platform structure in accordance with the invention;

FIGs. 5A-5D are schematic diagrams of the corresponding process flow and layer structure for a surface channel FET platform in accordance with the invention;

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure for a buried channel FET platform in accordance with the invention;

FIGs. 7A-7D are schematic diagrams of a process flow for a surface channel MOSFET in accordance with the invention;

FIGs. 8A and 8B are schematic block diagrams of surface channel devices with

protective layers;

FIGs. 9A and 9B are schematic block diagrams of surface channel devices with Si layers on Ge-rich layers for use in silicide formation;

FIGs. 10 is schematic diagram of a buried channel MOSFET after device isolation in accordance with the invention;

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention;

FIGs. 12A-12D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the top strained Si layer in accordance with the invention;

FIGs. 13A-13D are schematic diagrams of a process flow in the case of forming the surface channel MOSFET in the buried strained Si layer in accordance with the invention; and

FIGs. 14A and 14B are schematic diagrams of surface and buried channel devices with $Si_{1-y}Ge_y$ channels on a relaxed $Si_{1-z}Ge_z$ layer.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic block diagram of a structure 100 including a relaxed SiGe layer epitaxially grown on a Si substrate 102. In this structure, a compositionally graded buffer layer 104 is used to accommodate the lattice mismatch between the uniform SiGe layer 106 and the Si substrate. By spreading the lattice mismatch over a distance, the graded buffer minimizes the number of dislocations reaching the surface and thus provides a method for growing high-quality relaxed SiGe films on Si.

Any method of growing a high-quality, relaxed SiGe layer on Si will produce roughness on the surface of the SiGe layer in a well-known crosshatch pattern. This crosshatch pattern is typically a few hundred angstroms thickness over distances of microns. Thus, the crosshatch pattern is a mild, undulating surface morphology with respect to the size of the electron or hole. For that reason, it is possible to create individual devices that achieve enhancements over their control Si device counterparts. However, commercialization of these devices requires injection of the material into the Si CMOS process environment to achieve low cost, high performance targets. This processing environment requires that the material and device characteristics have minimal impact on the manufacturing process. The crosshatch pattern on the surface of the wafer is one limiting characteristic of relaxed SiGe on Si that affects the yield and the ease of manufacture. Greater planarity is desired for high yield and ease in

lithography.

The origin of the crosshatch pattern is the stress fields from the injected misfit dislocations. This effect is depicted by the exemplary structure 200 shown in FIG. 2. By definition, the dislocations must be introduced in order to accommodate the lattice-mismatch between the SiGe alloy and the Si substrate. The stress fields originate at the dislocations, and are terminated at the surface of the film. However, the termination at the surface creates crystal lattices that vary from place to place on the surface of the wafer. Since growth rate can be correlated to lattice constant size, different thicknesses of deposition occur at different points on the wafer. One may think that thick layer growth beyond the misfit dislocations will smooth the layer of these thickness differences. Unfortunately, the undulations on the surface have a relatively long wavelength; therefore, surface diffusion is typically not great enough to remove the morphology.

FIG. 3 is a table that displays surface roughness data for relaxed SiGe buffers produced by dislocation injection via graded SiGe layers on Si substrates. Note that the as-grown crosshatch pattern for relaxed $Si_{0.8}Ge_{0.2}$ buffers creates a typical roughness of approximately 7.9nm. This average roughness increases as the Ge content in the relaxed buffer is increased. Thus, for any SiGe layer that is relaxed through dislocation introduction during growth, the surface roughness is unacceptable for state-of-the-art fabrication facilities. After the process in which the relaxed SiGe is planarized, the average roughness is less than 2nm (typically 0.57nm), and after device layer deposition, the average roughness is 0.77nm with a 1.5μm regrowth thickness. Therefore, after the complete structure is fabricated, over one order of magnitude of roughness reduction can be achieved.

The regrowth device layers can be either greater than or less than the critical thickness of the regrowth layer. In general, in any lattice-mismatched epitaxial growth, thin layers can be deposited without fear of dislocation introduction at the interface. At a great enough thickness, any lattice-mismatch between the film and substrate will introduce misfit dislocations into the regrown heterostructure. These new dislocations can cause additional surface roughness. Thus, if the lattice-mismatch between the regrowth device layers and relaxed SiGe buffer is too great, the effort of planarizing the relaxed SiGe may be lost since massive dislocation introduction will roughen the surface.

There are two distinct possibilities with respect to the regrowth thickness and the quality of surface. If the regrowth layers are very thin, then exact lattice matching of the

regrowth layer composition and the relaxed buffer composition is not necessary. In this case, the surface roughness will be very low, approximately equal to the post-planarization flatness. However, in many applications for devices, the regrowth layer thickness will be 1-2μm or more. For a 1% difference in Ge concentration between the relaxed SiGe and the regrowth layer, the critical thickness is approximately 0.5μm. Thus, if optimal flatness is desired, it is best to keep the regrowth layer below approximately 0.5μm unless excellent control of the uniformity of Ge concentration across the wafer is achieved. Although this composition matching is achievable in state-of-the-art tools, FIG. 3 shows that less precise matching, i.e., within 2% Ge, results in misfit dislocation introduction and introduction of a new crosshatch pattern. However, because the lattice mismatch is so small, the average roughness is still very low, approximately 0.77nm. Thus, either lattice-matching or slight mismatch will result in excellent device layer surfaces for processing.

It is also noted that the relaxed SiGe alloy with surface roughness may not necessarily be a uniform composition relaxed SiGe layer on a graded composition layer. Although this material layer structure has been shown to be an early example of high quality relaxed SiGe, there are some disadvantages to this structure. For example, SiGe alloys possess a much worse coefficient of thermal conductivity than pure Si. Thus, for electronic devices located at the surface, it may be relatively difficult to guide the heat away from the device areas due to the thick graded composition layer and uniform composition layer.

Another exemplary embodiment of the invention, shown in FIGs. 4A-4D, solves this problem and creates a platform for high power SiGe devices. FIGs. 4A–4D show an exemplary process flow and resulting platform structure in accordance with the invention. The structure is produced by first forming a relaxed uniform SiGe alloy 400 via a compositionally graded layer 402 on a Si substrate 404. The SiGe layer 400 is then transferred to a second Si substrate 406 using conventional bonding. For example, the uniform SiGe alloy 400 on the graded layer 402 can be planarized to remove the crosshatch pattern, and that relaxed SiGe alloy can be bonded to the Si wafer. The graded layer 402 and the original substrate 404 can be removed by a variety of conventional processes. For example, one process is to grind the original Si substrate away and selectively etch to the SiGe, either by a controlled dry or wet etch, or by embedding an etch stop layer. The end result is a relaxed SiGe alloy 400 on Si without the thick graded layer. This structure is more suited for high power applications since the heat can be conducted away from the SiGe layer more efficiently. The bond and substrate removal technique can also be used to produce SiGe on insulator substrates, or SGOI. An SGOI

wafer is produced using the same technique shown in FIGs. 4A-4D; however, the second substrate is coated with a SiO_2 layer before bonding. In an alternative embodiment, both wafers can be coated with SiO_2 to enable oxide-to-oxide bonding. The resulting structure after substrate removal is a high quality, relaxed SiGe layer on an insulating film. Devices built on this platform can utilize the performance enhancements of both strained Si and the SOI architecture.

It will be appreciated that in the scenario where the SiGe layer is transferred to another host substrate, one may still need to planarize before regrowing the device layer structure. The SiGe surface can be too rough for state of the art processing due to the substrate removal technique. In this case, the relaxed SiGe is planarized, and the device layers are regrown on top of the high-quality relaxed SiGe surface.

Planarization of the surface via mechanical or other physical methods is required to flatten the surface and to achieve CMOS-quality devices. However, the field effect transistors (FETs) that allow for enhanced digital and analog circuits are very thin, and thus would be removed by the planarization step. Thus, a first part of the invention is to realize that relaxed SiGe growth and planarization, followed by device layer regrowth, is key to creating a high-performance, high yield enhanced CMOS platform. FIGs. 5 and 6 show the process sequence and regrowth layers required to create embodiments of surface channel and buried channel FETs, respectively.

FIGs. 5A-5D are schematic diagrams of a process flow and resulting layer structure in accordance with the invention. FIG. 5A shows the surface roughness 500, which is typical of a relaxed SiGe alloy 502 on a substrate 504, as an exaggerated wavy surface. Note that the substrate is labeled in a generic way, since the substrate could itself be Si, a relaxed compositionally graded SiGe layer on Si, or another material in which the relaxed SiGe has been transferred through a wafer bonding and removal technique. The relaxed SiGe alloy 502 is planarized (FIG. 5B) to remove the substantial roughness, and then device regrowth layers 506 are epitaxially deposited (FIG. 5C). It is desirable to lattice-match the composition of the regrowth layer 506 as closely as possible to the relaxed SiGe 502; however, a small amount of mismatch and dislocation introduction at the interface is tolerable since the surface remains substantially planar. For a surface channel device, a strained Si layer 508 of thickness less than 0.1 μm is then grown on top of the relaxed SiGe 502 with an optional sacrificial layer 510, as shown in FIG. 5D. The strained layer 508 is the layer that will be used as the channel in the final CMOS devices.

FIGs. 6A-6D are schematic diagrams of the corresponding process flow and layer structure

for a buried channel FET platform in accordance with the invention. In this structure, the regrowth layers 606 include a lattice matched SiGe layer 602, a strained Si channel layer 608 with a thickness of less than 0.05μm, a SiGe separation or spacer layer 612, a Si gate oxidation layer 614, and an optional sacrificial layer 610 used to protect the heterostructure during the initial device processing steps.

Once the device structure has been deposited, the rest of the process flow for device fabrication is very similar to that of bulk Si. A simplified version of the process flow for a surface channel MOSFET in accordance with the invention is shown in FIGs. 7A-7D. This surface channel MOSFET contains a relaxed SiGe layer 700 and a strained Si layer 702. The device isolation oxide 704, depicted in FIG. 7A, is typically formed first. In this step, the SiN layer 706, which is on top of a thin pad oxide layer 708, serves as a hard mask for either local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Both techniques use a thick oxide (relative to device dimensions) to provide a high threshold voltage between devices; however, STI is better suited for sub-quarter-micron technologies. Figure 7B is a schematic of the device area after the gate oxide 716 growth and the shallow-source drain implant. The implant regions 710 are self-aligned by using a poly-Si gate 712 patterned with photoresist 714 as a masking layer. Subsequently, deep source-drain implants 718 are positioned using conventional spacer 720 formation and the device is electrically contacted through the formation of silicide 722 at the gate and silicide/germanides 724 at the source and drain (Figure 7C). Figure 7D is a schematic of the device after the first level of metal interconnects 726 have been deposited and etched.

Since there are limited-thickness layers on top of the entire structure, the removal of surface material during processing becomes more critical than with standard Si. For surface channel devices, the structure that is regrown consists primarily of nearly lattice-matched SiGe, and a thin surface layer of strained Si. Many of the processes that are at the beginning of a Si fabrication sequence strip Si from the surface. If the processing is not carefully controlled, the entire strained Si layer can be removed before the gate oxidation. The resulting device will be a relaxed SiGe channel FET and thus the benefits of a strained Si channel will not be realized.

A logical solution to combat Si removal during initial processing is to make the strained Si layer thick enough to compensate for this removal. However, thick Si layers are not possible for two reasons. First, the enhanced electrical properties originate from the fact that the Si is strained and thick layers experience strain relief through the introduction of misfit dislocations. Second, the misfit dislocations themselves are

undesirable in significant quantity, since they can scatter carriers and increase leakage currents in junctions.

In order to prevent removal of strained Si layers at the surface, the cleaning procedures before gate oxidation must be minimized and/or protective layers must be applied. Protective layers are useful since their removal can be carefully controlled. Some examples of protective layers for surface channel devices are shown in FIGS. 8A and 8B. FIG. 8A shows a strained Si heterostructure of a relaxed SiGe layer 800 and a strained Si channel layer 802 protected by a surface layer 804 of SiGe. The surface SiGe layer 804 should have a Ge concentration similar to that of the relaxed SiGe layer 800 below, so that the thickness is not limited by critical thickness constraints. During the initial cleans, the SiGe sacrificial layer is removed instead of the strained Si channel layer. The thickness of the sacrificial layer can either be tuned to equal the removal thickness, or can be made greater than the removal thickness. In the latter case, the excess SiGe can be selectively removed before the gate oxidation step to reveal a clean, strained Si layer at the as grown thickness. If the particular fabrication facility prefers a Si terminated surface, a sacrificial Si layer may be deposited on top of the SiGe sacrificial cap layer.

FIG. 8B shows a structure where a layer 806 of SiO_2 and a surface layer 808 of either a poly-crystalline or an amorphous material are used as protective layers. In this method, an oxide layer is either grown or deposited after the epitaxial growth of the strained Si layer. Subsequently, a polycrystalline or amorphous layer of Si, SiGe, or Ge is deposited. These semiconductor layers protect the strained-Si layer in the same manner as a SiGe cap during the processing steps before gate oxidation. Prior to gate oxidation, the poly/amorphous and oxide layers are selectively removed. Although the sacrificial layers are shown as protection for a surface channel device, the same techniques can be employed in a buried channel heterostructure.

Another way in which conventional Si processing is modified is during the source-drain silicide-germanide formation (FIG. 7C). In conventional Si processing, a metal (typically Ti, Co, or Ni) is reacted with the Si and, through standard annealing sequences, low resistivity silicides are formed. However, in this case, the metal reacts with both Si and Ge simultaneously. Since the silicides have much lower free energy than the germanides, there is a tendency to form a silicide while the Ge is expelled. The expelled germanium creates agglomeration and increases the resistance of the contacts. This increase in series resistance offsets the benefits of the extra drive current from the heterostructure, and negates the advantages of the structure.

Ti and Ni can form phases in which the Ge is not rejected severely, thus allowing the formation of a good contact. Co is much more problematic. However, as discussed above for the problem of Si removal, a protective layer(s) at the device epitaxy stage can be applied instead of optimizing the SiGe-metal reaction. For example, the strained Si that will become the surface channel can be coated with a high-Ge-content SiGe alloy (higher Ge content than the initial relaxed SiGe), followed by strained Si. Two approaches are possible using these surface contact layers. Both methods introduce thick Si at the surface and allow the conventional silicide technology to be practiced without encountering the problems with SiGe-metal reactions.

The first approach, shown on a surface channel heterostructure 900 in FIG. 9A, uses a Ge-rich layer 906 thin enough that it is substantially strained. The layer 906 is provided on a strained Si channel layer 904 and relaxed SiGe layer 902. In this case, if a subsequent Si layer 908 is beyond the critical thickness, the compressive Ge-rich layer 906 acts as a barrier to dislocations entering the strained Si channel 904. This barrier is beneficial since dislocations do not adversely affect the silicide process; thus, their presence in the subsequent Si layer 908 is of no consequence. However, if the dislocations were to penetrate to the channel, there would be adverse effects on the device.

A second approach, shown in FIG. 9B, is to allow a Ge-rich layer 910 to intentionally exceed the critical thickness, thereby causing substantial relaxation in the Ge-rich layer. In this scenario, an arbitrarily thick Si layer 912 can be applied on top of the relaxed Ge-rich layer. This layer will contain more defects than the strained channel, but the defects play no role in device operation since this Si is relevant only in the silicide reaction. In both cases, the process is free from the metal-SiGe reaction concerns, since the metal will react with Si-only.

Once the silicide contacts have been formed, the rest of the sequence is a standard Si CMOS process flow, except that the thermal budget is carefully monitored since, for example, the silicide-germanicide (if that option is used) typically cannot tolerate as high a temperature as the conventional silicide. A major advantage of using Si/SiGe FET heterostructures to achieve enhanced performance is the compatibility with conventional Si techniques. Many of the processes are identical to Si CMOS processing, and once the front-end of the process, i.e., the processing of the Si/SiGe heterostructure, is complete, the entire back-end process is uninfluenced by the fact that Si/SiGe lies below.

Even though the starting heterostructure for the buried channel device is different

from that of the surface channel device, its process flow is very similar to the surface channel flow shown in FIGs. 7A-7D. FIG. 10 is a schematic block diagram of a buried channel MOSFET structure 1000 after the device isolation oxide 1016 has been formed using a SiN mask 1014. In this case, the strained channel 1002 on a first SiGe layer 1010 is separated from the surface by the growth of another SiGe layer 1004, followed by another Si layer 1006. This Si layer is needed for the gate oxide 1008 since gate-oxide formation on SiGe produces a very high interface state density, thus creating non-ideal MOSFETs. One consequence of this Si layer, is that if it is too thick, a substantial portion of the Si layer will remain after the gate oxidation. Carriers can populate this residual Si layer, creating a surface channel in parallel with the desired buried channel and leading to deleterious device properties. Thus, the surface layer Si must be kept as thin as possible, typically less than 50Å and ideally in the range of 5-15Å.

Another added feature that is necessary for a buried channel device is the supply layer implant. The field experienced in the vertical direction when the device is turned on is strong enough to pull carriers from the buried channel 1002 and force them to populate a Si channel 1006 near the Si/SiO_2 interface 1012, thus destroying any advantage of the buried channel. Thus, a supply layer of dopant must be introduced either in the layer 1004 between the buried channel and the top Si layer 1006, or below the buried channel in the underlying SiGe 1010. In this way, the device is forced on with little or no applied voltage, and turned off by applying a voltage (depletion mode device).

FIG. 11 is a schematic flow of the process, for any heterostructure FET device deposited on relaxed SiGe, in accordance with the invention. The main process steps are shown in the boxes, and optional steps or comments are shown in the circles. The first three steps (1100,1102,1104) describe the fabrication of the strained silicon heterostructure. The sequence includes production of relaxed SiGe on Si, planarization of the SiGe, and regrowth of the device layers. Once the strained heterostructure is complete (1106), MOS fabrication begins with device isolation (1112) using either STI (1110) or LOCOS (1108). Before proceeding to the gate oxidation, buried channel devices undergo a supply and threshold implant (1114), and any protective layers applied to either a buried or surface channel heterostructure must be selectively removed (1116). The processing sequence after the gate oxidation (1118) is similar to conventional Si CMOS processing. These steps include gate deposition, doping, and definition (1120), self-aligned shallow source-drain implant (1122), spacer formation (1124), self-aligned deep source-drain implant (1126), salicide formation (1128), and pad isolation via metal deposition and etch

(1130). The steps requiring significant alteration have been discussed.

One particular advantage of the process of FIG. 11 is that it enables the use of surface channel and buried channel devices on the same platform. Consider FIGs. 12A-12D and FIGs. 13A-13D, which show a universal substrate layer configuration and a process that leads to the co-habitation of surface and buried channel MOSFETs on the same chip. The universal substrate is one in which both surface channel and buried channel devices can be fabricated. There are two possibilities in fabricating the surface channel device in this sequence, shown in FIGs. 12 and 13. The process flows for combining surface and buried channel are similar to the previous process described in FIG. 7. Therefore, only the critical steps involved in exposing the proper gate areas are shown in FIGs. 12 and 13.

FIGs. 12A and 13A depict the same basic heterostructure 1200,1300 for integrating surface channel and buried channel devices. There is a surface strained Si layer 1202,1302, a SiGe spacer layer 1204,1304, a buried strained Si layer 1206,1306, and a relaxed platform of SiGe 1208,1308. Two strained Si layers are necessary because the buried channel MOSFET requires a surface Si layer to form the gate oxide and a buried Si layer to form the device channel. The figures also show a device isolation region 1210 that separates the buried channel device area 1212,1312 from the surface channel device area 1214,1314.

Unlike the buried channel device, a surface channel MOSFET only requires one strained Si layer. As a result, the surface channel MOSFET can be fabricated either in the top strained Si layer, as shown in FIGs. 12B-12D, or the buried Si layer channel, as shown in FIGs. 13B-13D. FIG. 12B is a schematic diagram of a surface channel gate oxidation 1216 in the top Si layer 1202. In this scenario, a thicker top Si layer is desired, since after oxidation, a residual strained Si layer must be present to form the channel. FIG. 12B also shows a possible position for the buried channel supply implant 1218, which is usually implanted before the buried channel gate oxide is grown. Since the top Si layer is optimized for the surface channel device, it may be necessary to strip some of the top strained Si in the regions 1220 where buried channel devices are being created, as shown in FIG. 12C. This removal is necessary in order to minimize the surface Si thickness after gate oxide 1222 formation (FIG. 12D), and thus avoid the formation of a parallel device channel.

When a surface channel MOSFET is formed in the buried strained Si layer, the top strained Si layer can be thin, i.e., designed optimally for the buried channel MOSFET. In FIG. 13B, the top strained Si and SiGe layers are removed in the region 1312 where the

surface channel MOSFETs are formed. Because Si and SiGe have different properties, a range of selective removal techniques can be used, such as wet or dry chemical etching. Selective oxidation can also be used since SiGe oxidizes at much higher rates than Si, especially under wet oxidation conditions. FIG. 13C shows the gate oxidation 1314 of the surface channel device as well as the supply layer implant 1316 for the buried channel device. Finally, FIG. 13D shows the position of the buried channel gate oxide 1318. No thinning of the top Si layer is required prior to the oxidation since the epitaxial thickness is optimized for the buried channel device. Subsequent to these initial steps, the processing for each device proceeds as previously described.

Another key step in the process is the use of a localized implant to create the supply layer needed in the buried channel device. In a MOSFET structure, when the channel is turned on, large vertical fields are present that bring carriers to the surface. The band offset between the Si and SiGe that confines the electrons in the buried strained Si layer is not large enough to prevent carriers from being pulled out of the buried channel. Thus, at first, the buried channel MOSFET would appear useless. However, if enough charge were present in the top SiGe layer, the MOSFET would become a depletion-mode device, i.e. normally on and requiring bias to turn off the channel. In the surface/buried channel device platform, a supply layer implant can be created in the regions where the buried channel will be fabricated, thus easing process integration. If for some reason the supply layer implant is not possible, note that the process shown in FIG. 11 in which the surface channel is created on the buried Si layer is an acceptable process, since the dopant can be introduced into the top SiGe layer during epitaxial growth. The supply layer is then removed from the surface channel MOSFET areas when the top SiGe and strained Si layers are selectively etched away.

In the processes described in FIGs. 10, 12 and 13, it is assumed that the desire is to fabricate a buried channel MOSFET. If the oxide of the buried channel device is removed, one can form a buried channel device with a metal gate (termed a MODFET or HEMT). The advantage of this device is that the transconductance can be much higher since there is a decrease in capacitance due to the missing oxide. However, there are two disadvantages to using this device. First, all thermal processes after gate definition have to be extremely low temperature, otherwise the metal will react with the semiconductor, forming an alloyed gate with a very low, or non-existent, barrier. Related to this issue is the second disadvantage. Due to the low thermal budget, the source and drain formation and contacts are typically done before the gate definition. Inverting these steps prevents the gate from being self-aligned to the source and drain, thus increasing the series resistance between the

gate and the source and drain. Therefore, with a carefully designed buried channel MOSFET, the self-aligned nature can be a great advantage in device performance. Another benefit of the MOSFET structure is that the gate leakage is very low.

The combination of buried n-channel structures with n and p type surface channel MOSFETs has been emphasized heretofore. It is important to also emphasize that in buried n-channel devices as well as in surface channel devices, the channels need not be pure Si. $Si_{1-y}Ge_y$ channels can be used to increase the stability during processing. FIGs. 14A and 14B are schematic diagrams of surface 1400 and buried 1450 channel devices with $Si_{1-y}Ge_y$ channels 1402 on a relaxed $Si_{1-z}Ge_z$ layer 1404. The devices are shown after salicidation and thus contain a poly-Si gate 1410, gate oxide 1408, silicide regions 1412, spacers 1414, and doped regions 1416. In the surface channel device 1400, a thin layer 1406 of Si must be deposited onto the $Si_{1-y}Ge_y$ layer 1402 to form the gate oxide 1408, as previously described for buried channel devices. In the buried $Si_{1-y}Ge_y$ channel device 1450, the device layer sequence is unchanged and consists of a buried strained channel 1402, a SiGe spacer layer 1418, and a surface Si layer 1420 for oxidation.

To maintain tensile strain in the channel of an nMOS device, the lattice constant of the channel layer must be less than that of the relaxed SiGe layer, i.e., y must be less than z. Since n-channel devices are sensitive to alloy scattering, the highest mobilities result when the Ge concentration in the channel is low. In order to have strain on this channel layer at a reasonable critical thickness, the underlying SiGe should have a Ge concentration in the range of 10-50%.

Experimental data indicates that p channels are less sensitive to alloy scattering. Thus, surface MOSFETs with alloy channels are also possible. In addition, the buried channel devices can be p-channel devices simply by having the Ge concentration in the channel, y, greater than the Ge concentration in the relaxed SiGe alloy, z, and by switching the supply dopant from n-type to p-type. This configuration can be used to form Ge channel devices when $y = 1$ and $0.5 < z < 0.9$.

With the ability to mix enhancement mode surface channel devices (n and p channel, through implants as in typical Si CMOS technology) and depletion-mode buried channel MOSFETs and MODFETs, it is possible to create highly integrated digital/analog systems. The enhancement mode devices can be fabricated into high performance CMOS, and the regions of an analog circuit requiring the high performance low-noise depletion mode device can be fabricated in the buried channel regions. Thus, it is possible to construct optimal communication stages, digital processing stages, etc. on a single

platform. These different regions are connected electrically in the backend of the Si CMOS chip, just as transistors are connected by the back-end technology today. Thus, the only changes to the CMOS process are some parameters in the processes in the fabrication facility, and the new material, but otherwise, the entire manufacturing process is transparent to the change. Thus, the economics favor such a platform for integrated Si CMOS systems on chip.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A surface channel MOSFET comprising:
a relaxed planarized SiGe layer on a substrate;
a regrown $Si_{1-x}Ge_x$ layer with thickness h;
a Si channel layer;
a gate dielectric;
a polycrystalline semiconductor layer; and
a highly conductive gate layer.

2. The MOSFET of claim 1, wherein h is approximately 0.

3. The MOSFET of claim 1, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

4. The MOSFET of claim 1, wherein the substrate comprises Si.

5. The MOSFET of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

6. A surface channel MOSFET comprising:
a relaxed planarized SiGe layer on a substrate;
a regrown $Si_{1-x}Ge_x$ layer with thickness h;
a Ge channel layer;
a Si layer;
a gate dielectric;
a polycrystalline semiconductor layer; and
a highly conductive gate layer.

7. The MOSFET of claim 6, wherein h is approximately 0.

8. The MOSFET of claim 6, wherein the thickness of the Si layer is less than 5nm.

9. The MOSFET of claim 6, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

10. The MOSFET of claim 6, wherein the substrate comprises Si.

11. The MOSFET of claim 6, wherein the substrate comprises Si with a layer of SiO_2.

12. A buried channel MOSFET comprising:
a relaxed planarized SiGe layer on a substrate;
a regrown $Si_{1-x}Ge_x$ layer with thickness h;
a Si channel layer;
a $Si_{1-y}Ge_y$ layer;
a second Si layer;
a gate dielectric;
a polycrystalline semiconductor layer; and
a highly conductive gate metal layer.

13. The MOSFET of claim 12, wherein h is approximately 0.

14. The MOSFET of claim 12, wherein the thickness of the second Si layer is less than 5nm.

15. The MOSFET of claim 12, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

16. The MOSFET of claim 15, wherein the supply layer dopants are implanted.

17. The MOSFET of claim 12, wherein the supply layer dopants are located below the Si channel layer.

18. The MOSFET of claim 17, wherein the supply layer dopants are implanted.

19. The MOSFET of claim 12, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

20. The MOSFET of claim 12, wherein the substrate comprises Si.

21. The MOSFET of claim 12, wherein the substrate comprises Si with a layer

of SiO_2.

22. A buried channel FET comprising:
a relaxed planarized SiGe layer on a substrate;
a regrown $Si_{1-x}Ge_x$ layer with thickness h;
a Si channel layer;
a $Si_{1-y}Ge_y$ layer;
a second Si layer; and
a highly conductive gate layer.

23. The FET of claim 22, wherein h is approximately 0.

24. The FET of claim 22, wherein the thickness of the second Si layer is less than 5nm.

25. The FET of claim 22, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

26. The FET of claim 25, wherein the supply layer dopants are implanted.

27. The FET of claim 22, wherein the supply layer dopants are located below the Si channel layer.

28. The FET of claim 27, wherein the supply layer dopants are implanted.

29. The FET of claim 22, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

30. The FET of claim 22, wherein the substrate comprises Si.

31. The FET of claim 22, wherein the substrate comprises Si with a layer of SiO_2.

32. A method of fabricating a surface channel MOSFET comprising:
providing a relaxed SiGe layer on a substrate;
planarizing said relaxed SiGe layer;
providing a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer;

providing a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer;

providing a gate dielectric on said Si channel layer;

providing a polycrystalline semiconductor layer on said gate dielectric; and

providing a highly conductive gate layer on said polycrystalline semiconductor layer.

33. The method of claim 32, wherein h is approximately 0.

34. The method of claim 32, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

35. The method of claim 32, wherein the substrate comprises Si.

36. The method of claim 32, wherein the substrate comprises Si with a layer of SiO_2.

37. A method of fabricating a surface channel MOSFET comprising:

providing a relaxed SiGe layer on a substrate;

planarizing said relaxed SiGe layer;

providing a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer;

providing a Ge channel layer on said regrown $Si_{1-x}Ge_x$ layer;

providing a Si layer on said Ge channel layer;

providing a gate dielectric on said Si layer;

a polycrystalline semiconductor layer; and

a highly conductive gate layer.

38. The method of claim 37, wherein h is approximately 0.

39. The method of claim 37, wherein the thickness of the Si layer is less than 5nm.

40. The method of claim 37, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

41. The method of claim 37, wherein the substrate comprises Si.

42. The method of claim 37, wherein the substrate comprises Si with a layer of

SiO_2.

43. A method of fabricating a buried channel MOSFET comprising:
providing a relaxed SiGe layer on a substrate;
planarizing said relaxed SiGe layer;
providing a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer;
providing a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer;
providing a $Si_{1-y}Ge_y$ layer on said Si channel layer;
providing a Si layer on said $Si_{1-y}Ge_y$ layer;
providing a gate dielectric on said Si layer;
providing a polycrystalline semiconductor layer on said gate dielectric; and
providing a highly conductive gate metal layer on said polycrystalline semiconductor layer.

44. The method of claim 43, wherein h is approximately 0.

45. The method of claim 43, wherein the thickness of the Si layer is less than 5nm.

46. The method of claim 43, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

47. The method of claim 46, wherein the supply layer dopants are implanted.

48. The method of claim 43, wherein the supply layer dopants are located below the Si channel layer.

49. The method of claim 48, wherein the supply layer dopants are implanted.

50. The method of claim 43, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

51. The method of claim 43, wherein the substrate comprises Si.

52. The method of claim 43, wherein the substrate comprises Si with a layer of SiO_2.

53. A method of fabricating a buried channel FET comprising:

providing a relaxed SiGe layer on a substrate;

planarizing said relaxed SiGe layer;

providing a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer;

providing a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer;

providing a $Si_{1-y}Ge_y$ layer on said Si channel layer;

providing a Si layer on said $Si_{1-y}Ge_y$ layer; and

providing a highly conductive gate layer on said Si layer.

54. The method of claim 53, wherein h is approximately 0.

55. The method of claim 53, wherein the thickness of the second Si layer is less than 5nm.

56. The method of claim 53, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

57. The method of claim 56, wherein the supply layer dopants are implanted.

58. The method of claim 53, wherein the supply layer dopants are located below the Si channel layer.

59. The method of claim 58, wherein the supply layer dopants are implanted.

60. The method of claim 53, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

61. The method of claim 53, wherein the substrate comprises Si.

62. The method of claim 53, wherein the substrate comprises Si with a layer of SiO_2.

63. A method of fabricating a surface channel MOSFET on a heterostructure, said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer, and a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer, said method comprising:

providing a gate dielectric on said Si channel layer;

providing a polycrystalline semiconductor layer on said gate dielectric; and

providing a highly conductive gate layer on said polycrystalline semiconductor layer.

64. The method of claim 63, wherein h is approximately 0.

65. The method of claim 63, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

66. The method of claim 63, wherein the substrate comprises Si.

67. The method of claim 63, wherein the substrate comprises Si with a layer of SiO_2.

68. A method of fabricating a surface channel MOSFET on a heterostructure, said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer, a Ge channel layer on said regrown $Si_{1-x}Ge_x$ layer, and a Si layer on said Ge channel layer, said method comprising:

providing a gate dielectric on said Si layer;

providing a polycrystalline semiconductor layer; and

providing a highly conductive gate layer.

69. The method of claim 68, wherein h is approximately 0.

70. The method of claim 68, wherein the thickness of the Si layer is less than 5nm.

71. The method of claim 68, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

72. The method of claim 68, wherein the substrate comprises Si.

73. The method of claim 68, wherein the substrate comprises Si with a layer of SiO_2.

74. A method of fabricating a buried channel MOSFET on a heterostructure, said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer, a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ layer on said Si channel layer, and a Si layer on said $Si_{1-y}Ge_y$ layer, said method comprising:

providing a gate dielectric on said Si layer;

providing a polycrystalline semiconductor layer on said gate dielectric; and

providing a highly conductive gate metal layer on said polycrystalline semiconductor layer.

75. The method of claim 74, wherein h is approximately 0.

76. The method of claim 74, wherein the thickness of the Si layer is less than 5nm.

77. The method of claim 74, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

78. The method of claim 77, wherein the supply layer dopants are implanted.

79. The method of claim 74, wherein the supply layer dopants are located below the Si channel layer.

80. The method of claim 79, wherein the supply layer dopants are implanted.

81. The method of claim 74, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

82. The method of claim 74, wherein the substrate comprises Si.

83. The method of claim 74, wherein the substrate comprises Si with a layer of SiO_2.

84. A method of fabricating a buried channel FET on a heterostructure, said heterostructure including a planarized relaxed SiGe layer on a substrate, a regrown $Si_{1-x}Ge_x$ layer with thickness h on said planarized relaxed SiGe layer, a Si channel layer on said regrown $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ layer on said Si channel layer, and a Si layer on said Si_{1-}

$_yGe_y$ layer, said method comprising:

providing a highly conductive gate layer on said Si layer.

85. The method of claim 84, wherein h is approximately 0.

86. The method of claim 84, wherein the thickness of the second Si layer is less than 5nm.

87. The method of claim 84, wherein supply layer dopants are located in the $Si_{1-y}Ge_y$ layer.

88. The method of claim 87, wherein the supply layer dopants are implanted.

89. The method of claim 84, wherein the supply layer dopants are located below the Si channel layer.

90. The method of claim 89, wherein the supply layer dopants are implanted.

91. The method of claim 84, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

92. The method of claim 84, wherein the substrate comprises Si.

93. The method of claim 84, wherein the substrate comprises Si with a layer of SiO_2.

94. A method of fabricating a semiconductor structure comprising:

providing a relaxed $Si_{1-x}Ge_x$ layer on a substrate;

planarizing said relaxed $Si_{1-x}Ge_x$ layer;

depositing a heterostructure on said planarized relaxed $Si_{1-x}Ge_x$ layer including at least one strained layer; and

configuring a semiconductor device on said heterostructure.

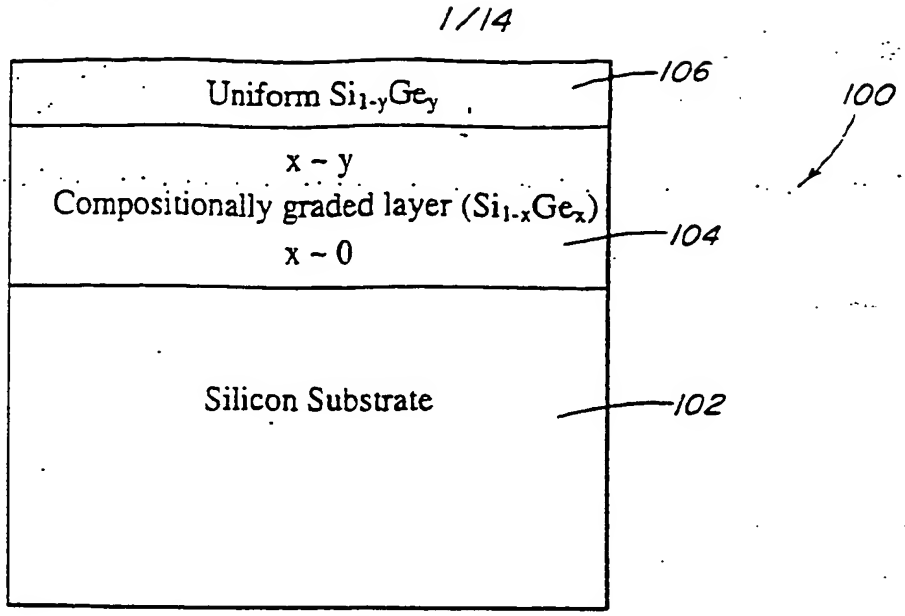

FIG. 1

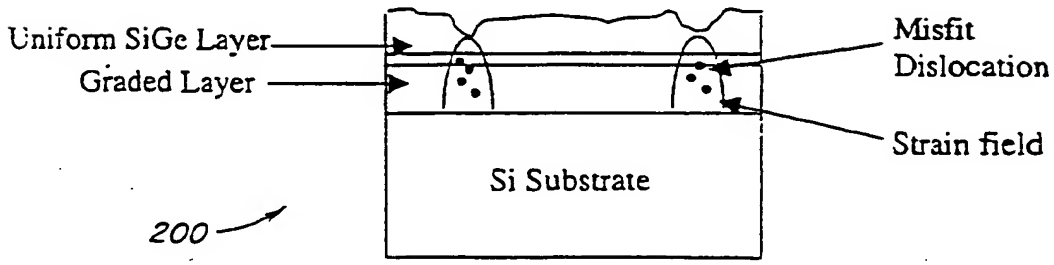

FIG. 2

Type of Surface	Average Roughness (nm)
As-grown graded composition relaxed SiGe	7.9
Planarized SiGe	0.57
Regrowth SiGe, lattice-matched	~0.6
Regrowth SiGe, slight mismatch, thickness =1.5μm	0.77

FIG. 3

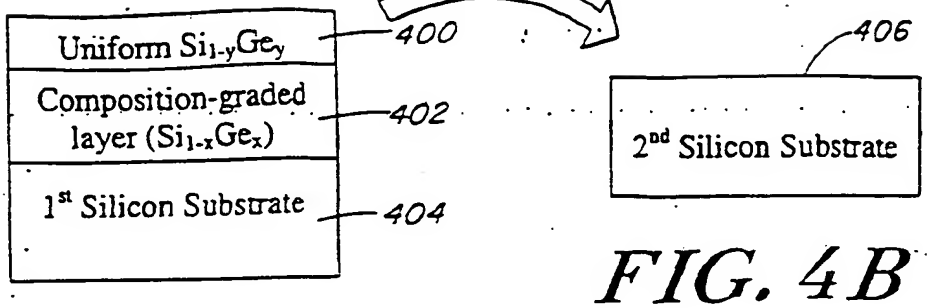

FIG. 4A

FIG. 4B

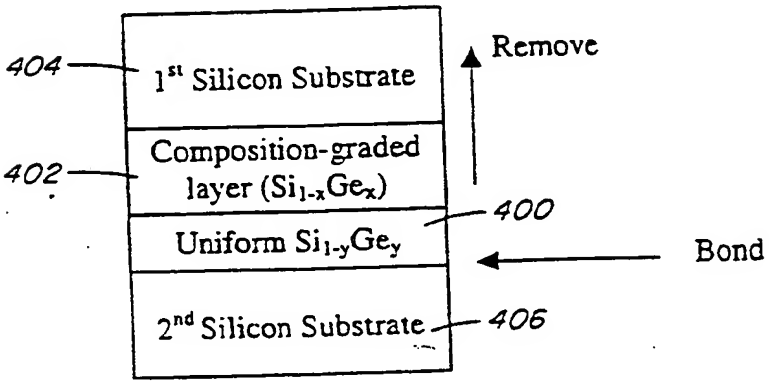

FIG. 4C

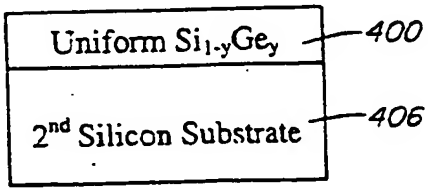

FIG. 4D

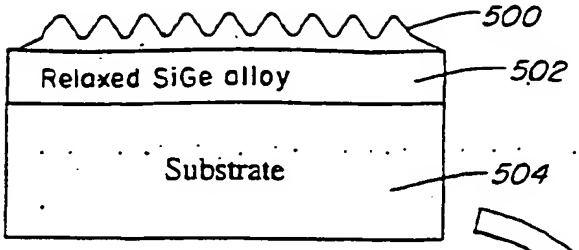

FIG. 5A

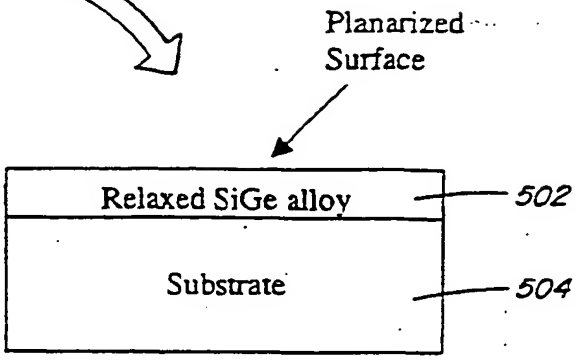

FIG. 5B

FIG. 5C

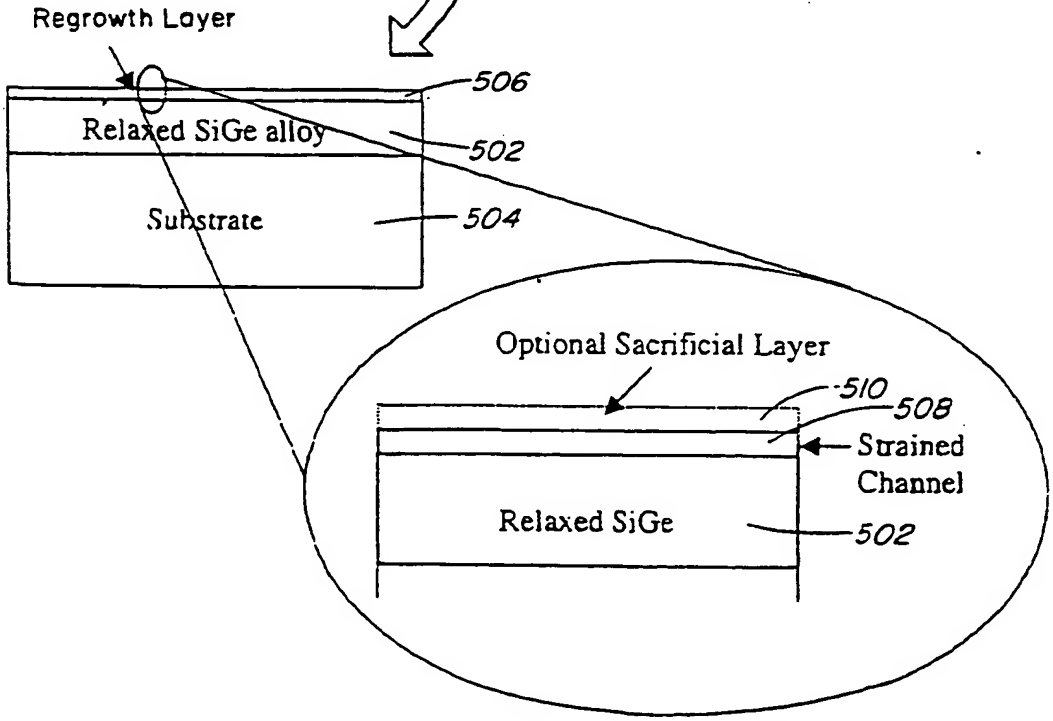

FIG. 5D

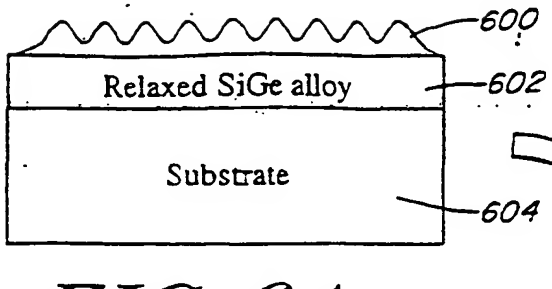

FIG. 6A

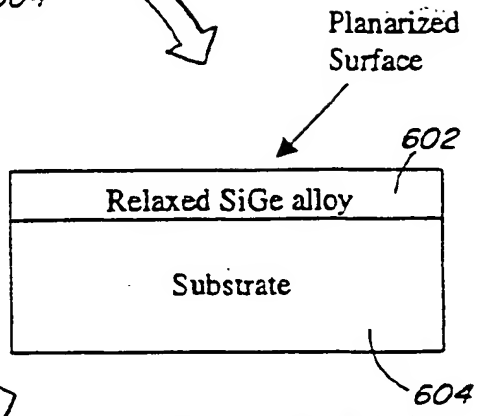

FIG. 6B

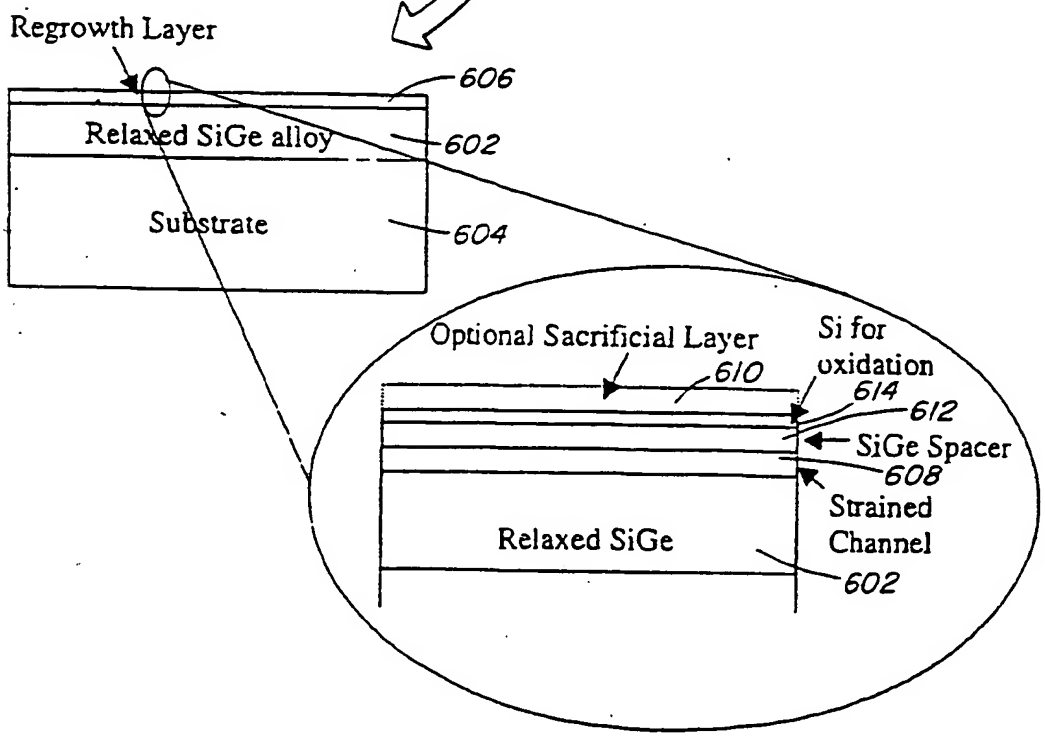

FIG. 6C

FIG. 6D

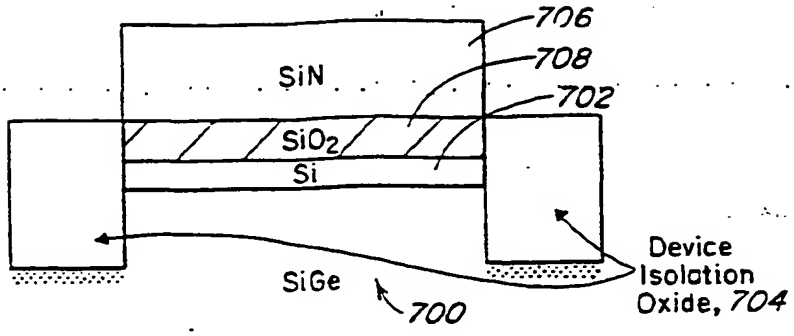
706
708
SiN
702
SiO_2
Si
Device
Isolation
Oxide, 704
SiGe
700

FIG. 7A

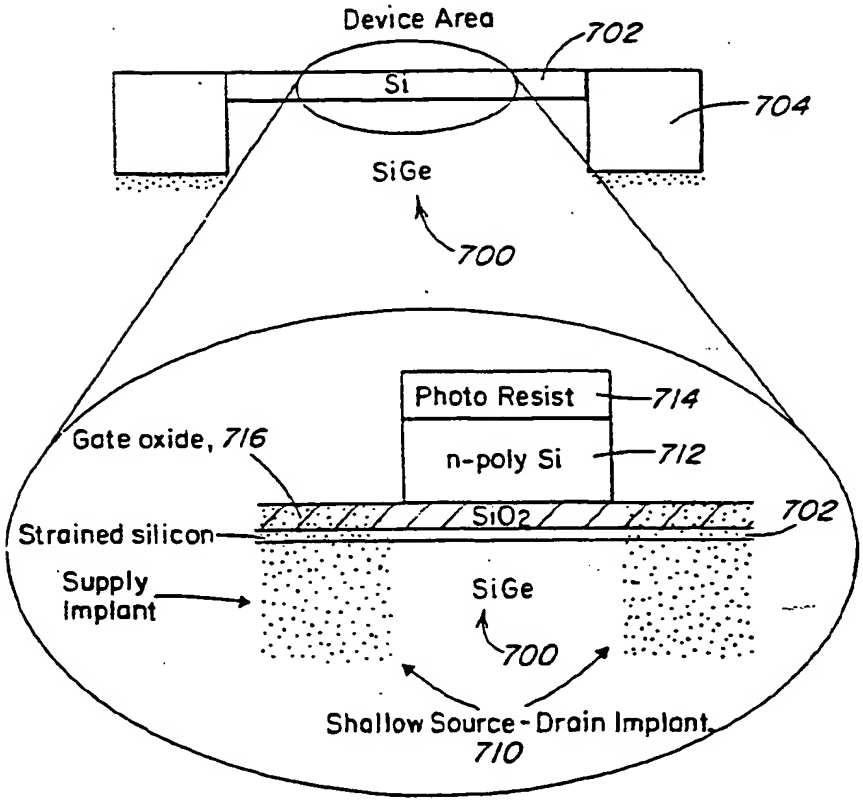
Device Area
702
Si
704
SiGe
700
Photo Resist
714
Gate oxide, 716
n-poly Si
712
SiO_2
702
Strained silicon
Supply
Implant
SiGe
700
Shallow Source-Drain Implant,
710

FIG. 7B

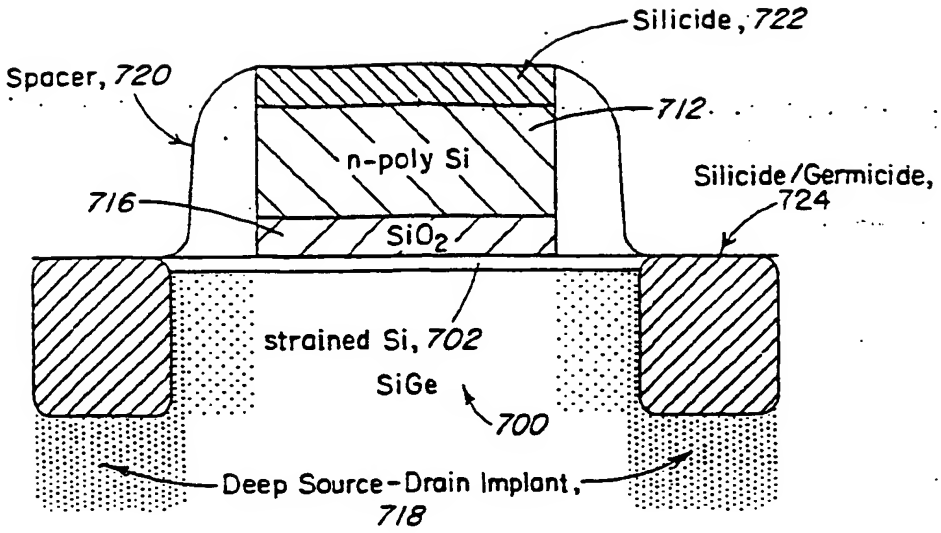
Silicide, 722
Spacer, 720
712
n-poly Si
Silicide/Germicide, 724
716
SiO_2
strained Si, 702
SiGe
700
Deep Source-Drain Implant, 718

FIG. 7C

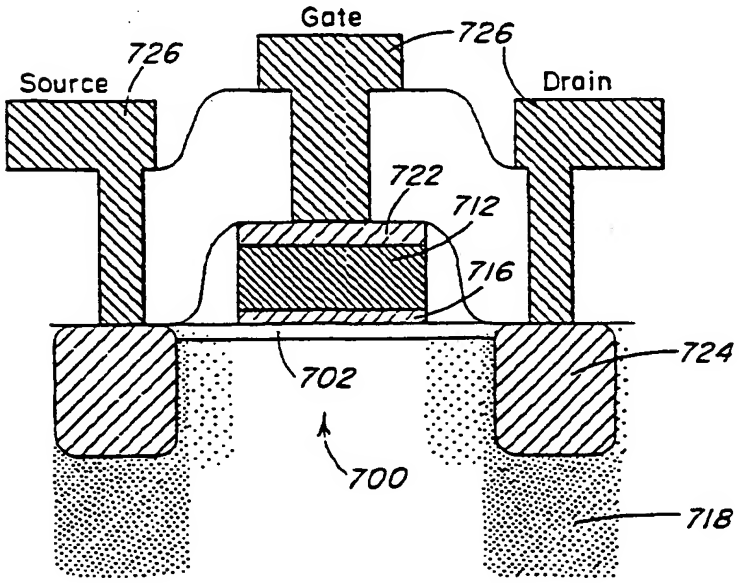
Gate
726
726
Source
Drain
722
712
716
724
702
700
718

FIG. 7D

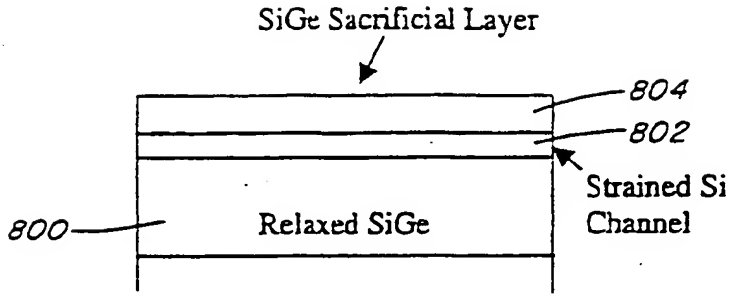
SiGe Sacrificial Layer
804
802
Strained Si
Channel
800
Relaxed SiGe

FIG. 8A

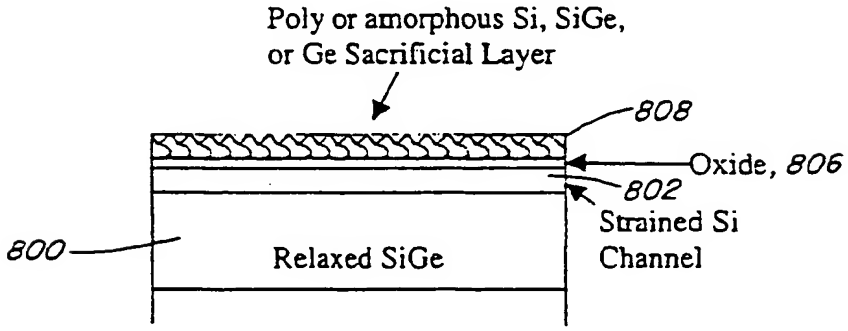
Poly or amorphous Si, SiGe,
or Ge Sacrificial Layer
808
Oxide, 806
802
Strained Si
Channel
800
Relaxed SiGe

FIG. 8B

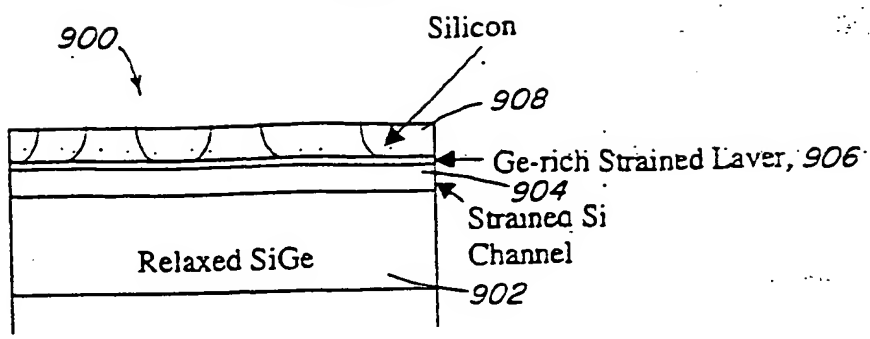

FIG. 9A

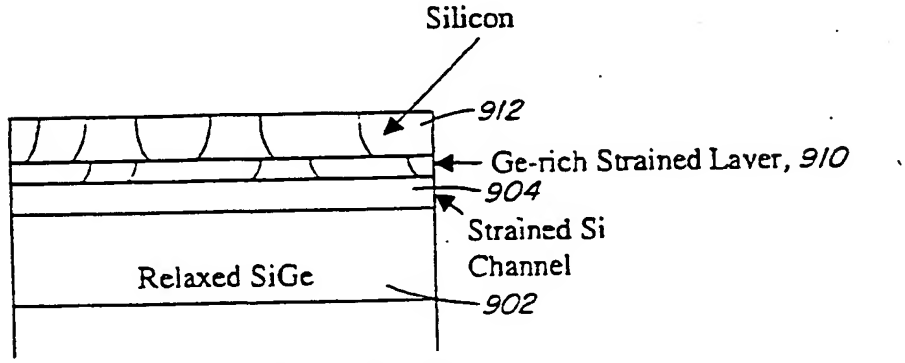

FIG. 9B

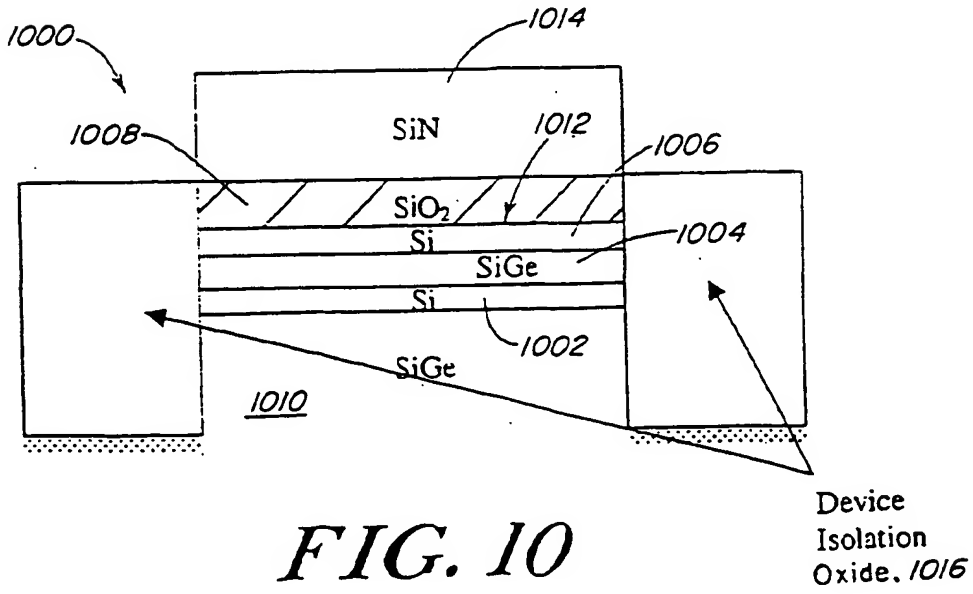

FIG. 10

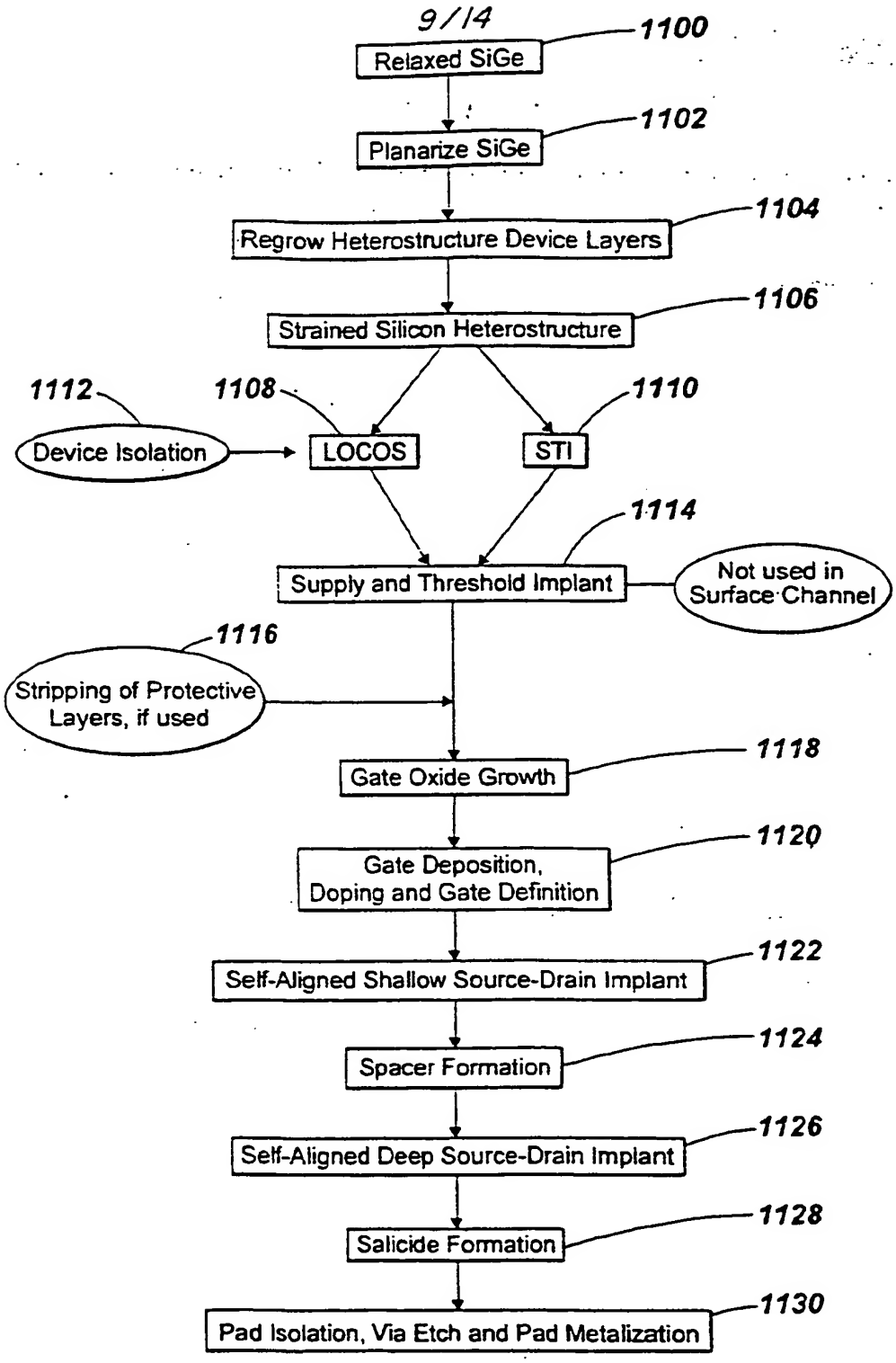
1100
Relaxed SiGe
1102
Planarize SiGe
1104
Regrow Heterostructure Device Layers
1106
Strained Silicon Heterostructure
1112
1108
1110
Device Isolation
LOCOS
STI
1114
Supply and Threshold Implant
Not used in Surface Channel
1116
Stripping of Protective Layers, if used
1118
Gate Oxide Growth
1120
Gate Deposition, Doping and Gate Definition
1122
Self-Aligned Shallow Source-Drain Implant
1124
Spacer Formation
1126
Self-Aligned Deep Source-Drain Implant
1128
Salicide Formation
1130
Pad Isolation, Via Etch and Pad Metalization

FIG. 11

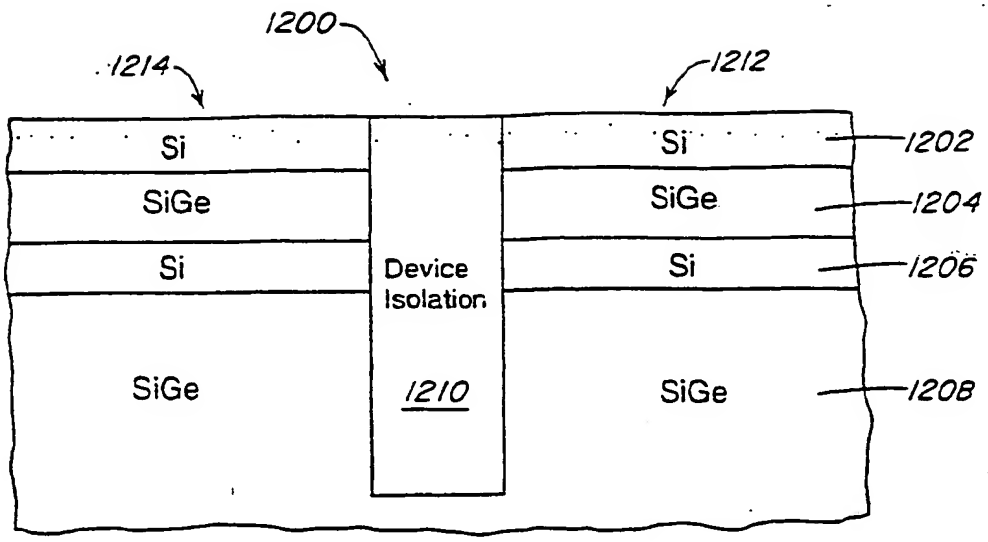

FIG. 12A

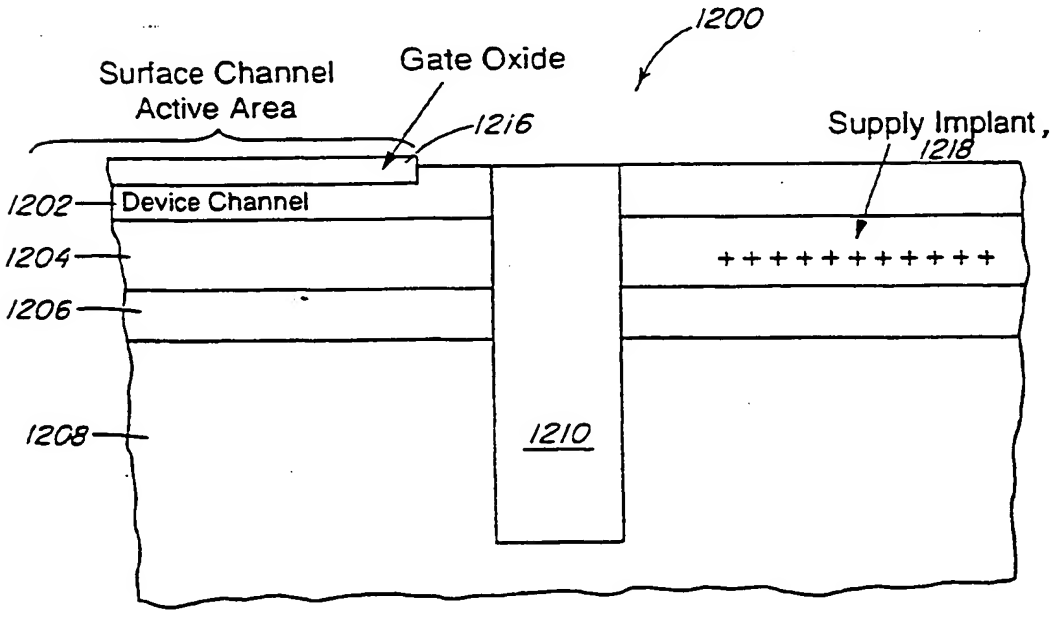

FIG. 12B

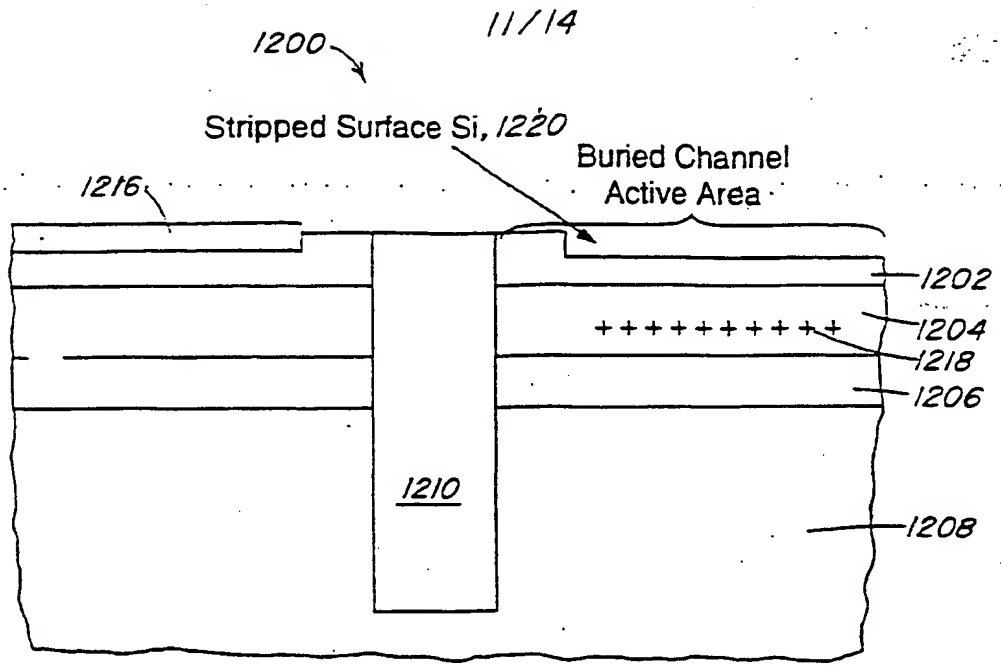

FIG. 12C

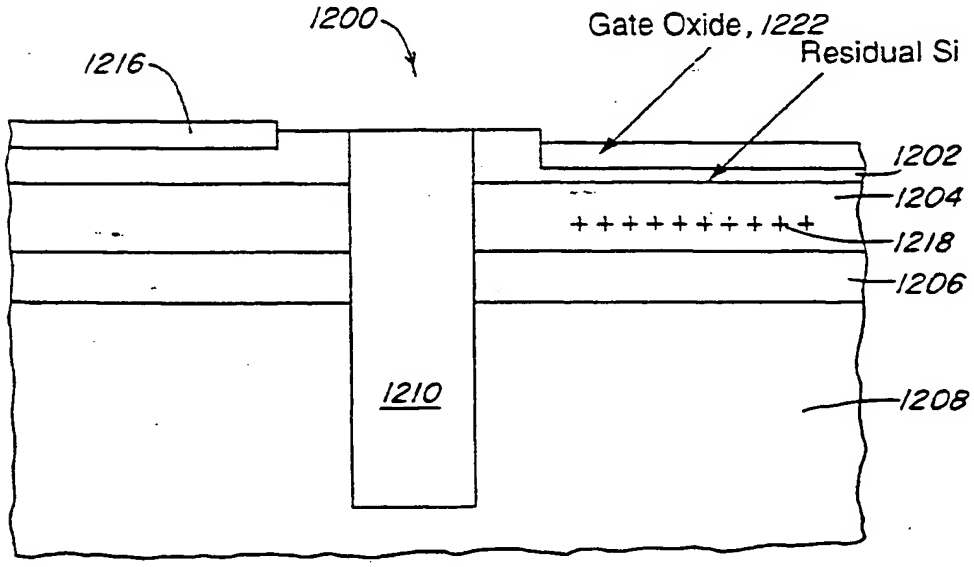

FIG. 12D

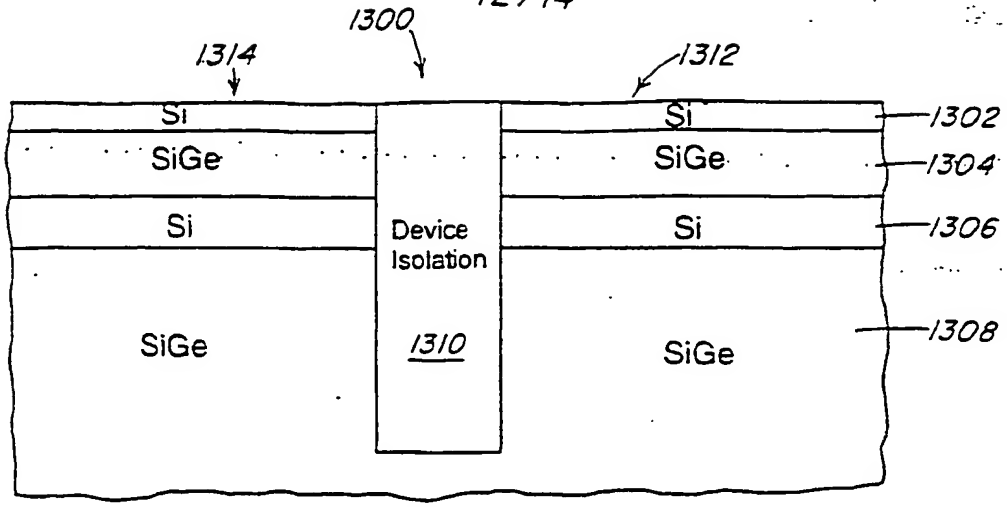

FIG. 13A

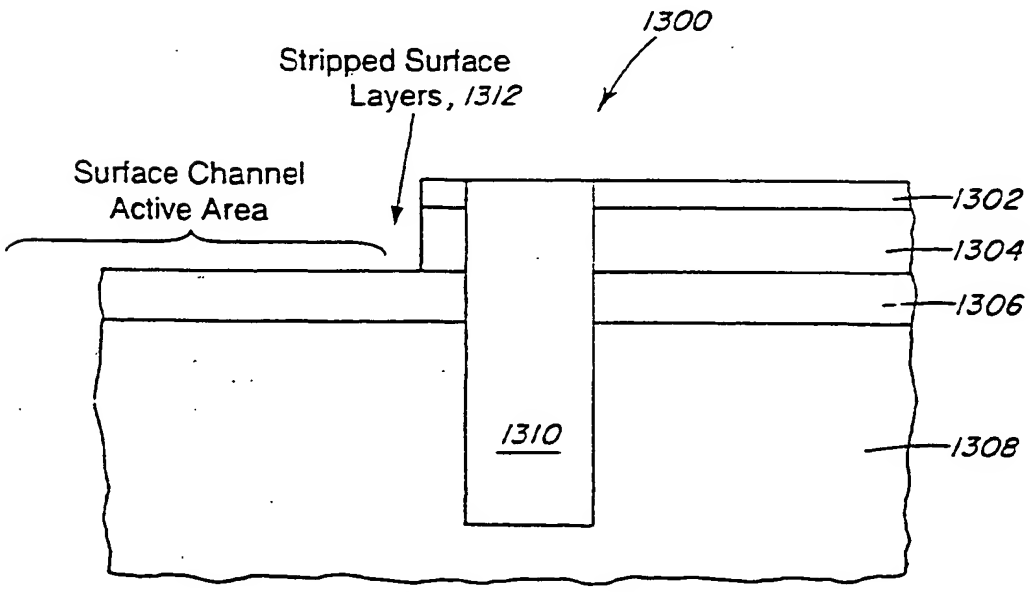

FIG. 13B

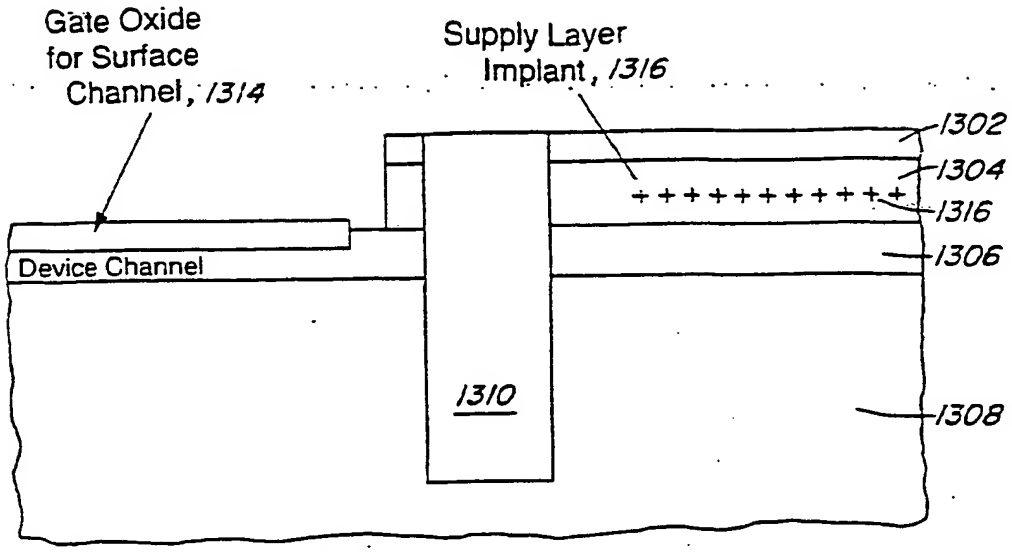

FIG. 13C

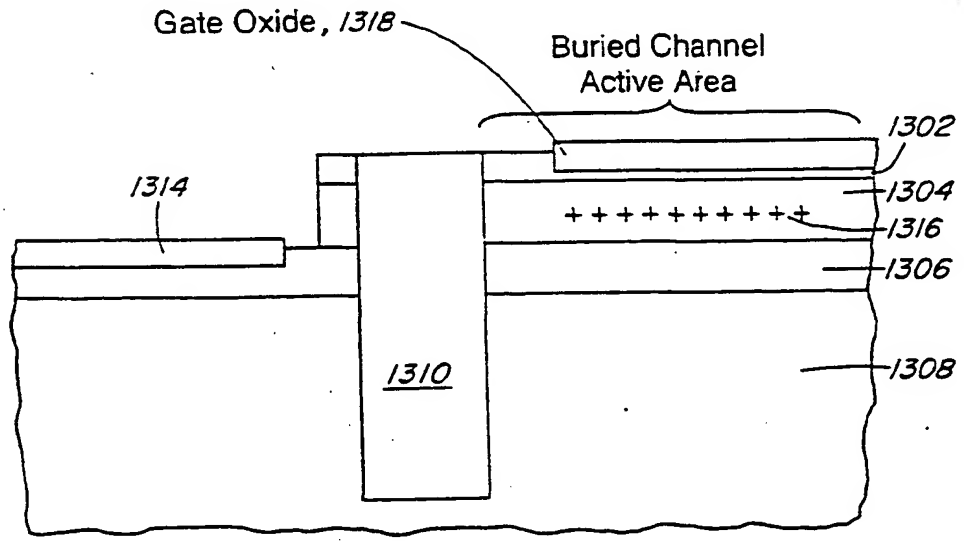

FIG. 13D

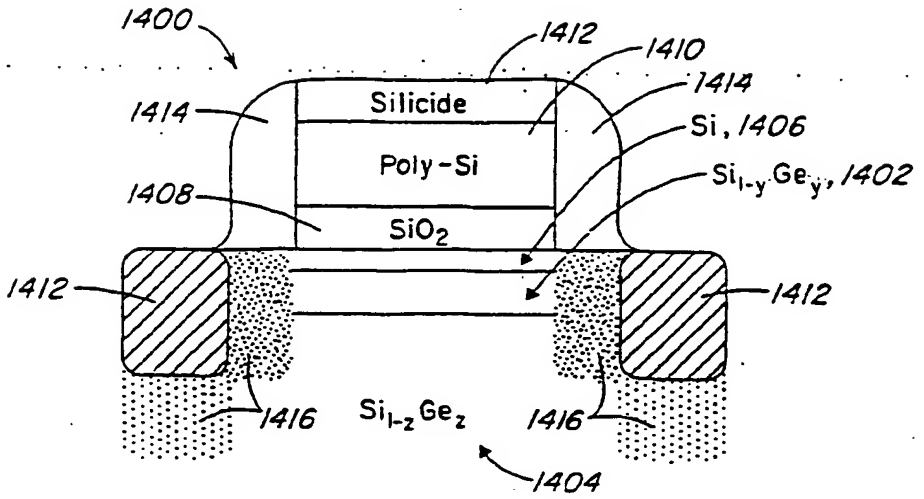

FIG. 14A

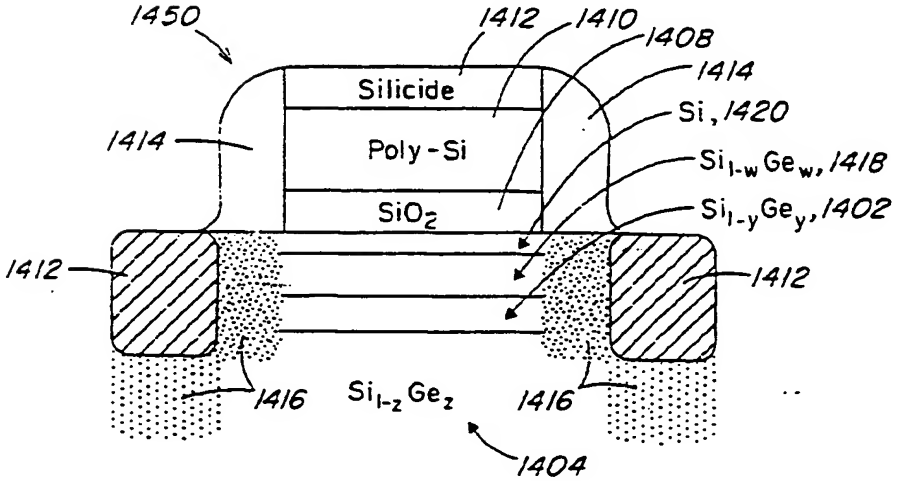

FIG. 14B

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/03688

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/10 H01L29/778 H01L21/335 H01L21/336 H01L29/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, COMPENDEX, INSPEC, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 891 769 A (HONG STELLA Q ET AL) 6 April 1999 (1999-04-06) column 2, line 37 -column 4, line 67; figures 1-3	1-5,94
Y	MAITI K ET AL: "STRAINED-SI HETEROSTRUCTURE FIELD EFFECT TRANSISTORS" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 13, no. 11, 1 November 1998 (1998-11-01), pages 1225-1246, XP000783138 ISSN: 0268-1242 page 1235 -page 1238; figures 13-18	1-93

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2002	05/07/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berthold, K

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/03688

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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X	HERZOG H-J ET AL: "SiGe-based FETs: buffer issues and device results" THIN SOLID FILMS, ELSEVIER-SEQUOIA S.A. LAUSANNE, CH, vol. 380, no. 1-2, 22 December 2000 (2000-12-22), pages 36-41, XP004226589 ISSN: 0040-6090 the whole document	22-30, 53-56, 58,60, 61, 84-87, 91,92,94
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A	WO 00 54338 A (IBM ;CHU JACK O (US)) 14 September 2000 (2000-09-14) abstract; figures 10-13	6-11
A	US 5 906 951 A (CHU JACK OON ET AL) 25 May 1999 (1999-05-25) abstract; figures 1-5	1-94
A	O'NEILL A G ET AL: "SIGE VIRTUAL SUBSTRATE N-CHANNEL HETEROJUNCTION MOSFETS" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 14, no. 9, September 1999 (1999-09), pages 784-789, XP000850219 ISSN: 0268-1242 page 785; figure 1	1-94
A	EP 0 683 522 A (IBM) 22 November 1995 (1995-11-22) column 9, line 22; figures 1-4	1-94

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/03688

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	KONIG U ET AL: "Design rules for n-type SiGe hetero FETs" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 41, no. 10, 1 October 1997 (1997-10-01), pages 1541-1547, XP004097077 ISSN: 0038-1101 abstract; figures 1,8	1-94

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Information on patent family members

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